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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,334	07/24/2003	Austin H. Lesea	X-1364 US	2275

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,334	LESEA ET AL	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *21-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/627334 Attorney's Docket #: X-1364 US
Filing Date: 7/24/03;

Applicant: Lesea et al.

Examiner: Alexander Williams

Applicant's election with traverse of the Species I of figures 3A-3D (claims 1-20) filed 6/19/06 is acknowledged.

Applicant's arguments in pages 1 and 2 is not found to be persuasive.

In the examination of claims Group I (claims 1 to 20) the Examiner would be interested in searching for the final structure of the semiconductor device claimed. In the examination of Group II (claims 21 to 27) the Examiner would be interested in the step claimed to achieve the semiconductor device claimed. Therefore, the two Groups would require a search in different art units and class. The two inventions are not sufficiently interrelated that similar art units would be examined for each group of claims. The Examiner would be examined for each group of claims. The Examiner would be unduly burdened to evaluate all claims fully on their merit at the full time.

Each of the Groups have searches in different art units and classes that would unduly burden the Examiner to evaluate all claims on their merit at the full time. This is not found persuasive because of the reasons detailed in the last Office action.

The requirement is still deemed proper and is therefore made FINAL.

This application contains claims 21-27 drawn to an invention non-elected with traverse. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR ∋ 1.144 & MPEP ∋ 821.01).

As to Applicant's arguments regarding the species election, the 3 species show different structures. Claims 1 and 11 are generic at this time.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: In paragraph [0034], line 4, widths "354" should probably be --344-- as shown in the drawing of figure 3D.

Appropriate correction is required.

The drawings are objected to because in figure 3C, the "spatial separation distance 301" is not shown in the drawing as described in paragraph [0033], line 3. In figure 3D, "the tapered signal line 401" is not shown in figure 3D as described in paragraph [0034], line 8.

Correction is required.

Claims are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Any of claims not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Miller et al. (U.S. Patent Application Publication # 2004/0266183 A1).

1. Miller et al. (figures 1a to 14d) specifically figure 11 show in an integrated circuit, a layer **1110** including a plurality of conductive wires **(layers of 1110 within 1120)**, the layer comprising: a horizontal surface of a first wire of the plurality of conductive wires **(layers of 1110 within 1120)** having a proximal end and a distal end, the proximal end having a first width, the distal end having a second width, the second width being less than the first width, the first wire taped from the proximal end to the distal end, the first wire further having a first substantially vertical surface; and a second wire of the plurality of conductive wires **(layers of 1110 within 1120)** spaced apart from the first wire, the second wire having a second substantially vertical surface, the first wire and the second wire are each horizontally disposed along side each first substantially vertical surface and the second substantially vertical surface, the one or more capacitor capacitances progressively reduced responsive to the first wire taper.

2. The layer, according to claim 1, Miller et al. further comprising at least one dielectric material disposed between the first substantially vertical surface and the second substantially vertical surface.
3. The layer, according to claim 1, Miller et al. show wherein the first wire is a signal wire.
4. The layer, according to claim 3, Miller et al. show wherein the second wire is a shielding wire.
5. The layer, according to claim 4, Miller et al. show wherein the first wire is tapered in progressively inward stepwise indentations away from the second wire along the first substantially vertical surface.
6. The layer, according to claim 5, Miller et al. show wherein the first wire is tapered in progressively inward stepwise indentations toward the second wire along another substantially vertical surface of the first wire.
7. The layer, according to claim 1, Miller et al. show wherein the first wire is a shielding wire, the shielding wire for a non-transitioning signal voltage, the non-transitioning signal voltage not transitioning form high to low and low to high logics levels during application of electrical energy to operate the integrated circuit.
8. The layer, according to claim 7, Miller et al. show wherein the second wire is a signal wire, the signal wire for a transitioning signal voltage, the transitioning signal voltage transitioning from high to low and low to high logic levels during application of the electrical energy to operate the integrated circuit.
9. The layer, according to claim 8, Miller et al. show wherein the first wire is continuously tapered away from the second wire along the first substantially vertical surface.
10. The layer, according to claim 8, Miller et al. show wherein the first wire is continuously tapered toward the second wire.
11. Miller et al. (figures 1a to 14d) specifically figure 11 show an integrated circuit conductive line, comprising: a plurality of loads **(layers of 1110 within 1120)** the plurality of loads progressively reduced responsive to progressively reduced parasitic capacitance; a plurality of taps, a tap of the plurality of taps located between a pair of loads of the plurality of loads.
12. The integrated circuit conductive line, according to claim 11, Miller et al. show wherein load capacitance at the tap is substantially less than the parasitic capacitance at the tap location from a portion of the plurality of loads.

13. The integrated circuit conductive lines, according to claim 12, Miller et al. show wherein the load capacitance comprises transistor gate capacitance.
14. The integrated circuit conductive line, according to claim 13, Miller et al. show wherein the transistor gate capacitance is from a transistor formed with sub-quarter micron lithography.
15. The integrated circuit conductive line, according to claim 14, Miller et al. show wherein the plurality of loads are provided using tapered signal line.
16. The integrated circuit conductive lien, according to claim 15, Miller et al. show wherein the tapered signal line has a minimum width of one micron.
17. The integrated circuit conductive line, according to claim 15, Miller et al. show wherein the tapered signal line is a clock signal line.
18. The integrated circuit conductive line, according to claim 15, Miller et al. show wherein the tapered signal line is a delay line.
19. The integrated circuit conductive line, according to claim 14, Miller et al. show wherein the plurality of loads are provided using a tapered shielding line.
20. The integrated circuit conductive line, according to claim 19, Miller et al. show wherein the tapered shielding line is either a ground line or a source voltage line.

[0005] Other advances in semiconductor manufacturing technology have lead to the integration of millions of transistors, each capable of switching at high speed. A consequence of incorporating so many fast switching transistors into an integrated circuit is an increase in power consumption during operation. One technique for increasing speed while reducing power consumption is to replace the traditional aluminum and aluminum alloy interconnects found on integrated circuits with a metal such as copper, which offers lower electrical resistance. Furthermore, because the resistance of copper is significantly less than that of aluminum, the cross-sectional area of a copper interconnect line, as compared to an aluminum interconnect line, may be made smaller without incurring increased signal propagation delays based on the resistance of the interconnect. Additionally, because the capacitance between two electrical nodes is a function of the overlap area between those nodes, using a smaller copper interconnect line results in a decrease in parasitic capacitance. In this way, replacing aluminum based interconnects with copper based interconnects provides, depending on the dimensions chosen, reduced resistance, reduced capacitance, or both. The use of copper

interconnects also provides greater immunity to electromigration. For all these reasons, manufacturers of integrated circuits find it desirable to include copper in their products.

[0027] The terms metal line, trace, wire, conductor, signal path and signaling medium are all related. The related terms listed above, are generally interchangeable, and appear in order from specific to general. In this field, metal lines are sometimes referred to as traces, wires, lines, interconnects or simply metal.

[0028] The terms contact and via both refer to structures for electrical connection of conductors from different interconnect levels. These terms are sometimes used in the art to describe both an opening in an insulator in which the structure will be completed, and the completed structure itself. For purposes of this disclosure contact and via refer to the completed structure.

[0029] The expression low k dielectric constant material refers to a material having a dielectric constant lower than the dielectric constant of silicon dioxide and specifically less than around 4.0. In embodiments of this invention the slurry disclosed is of particular use with low k dielectric materials such as SiOF, carbon doped oxide (CDO), porous oxide, and organic materials. Organic dielectric materials include for example organic polymers such as polyamide, parylene, polyarylether, polynaphtalene, or polyquinoline.

Claims 1 to 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Chiyoma (U.S. Patent # 4,679,088).

1. Chiyoma (figures 1 to 14) specifically figure 3 show in an integrated circuit, a layer including a plurality of conductive wires **4**, the layer comprising: a horizontal surface of a first wire of the plurality of conductive wires **4** having a proximal end **4b** and a distal end **4a**, the proximal end having a first width, the distal end having a second width, the second width being less than the first width, the first wire taped from the proximal end to the distal end, the first wire further having a first substantially vertical surface; and a second wire of the plurality of conductive wires **4** spaced apart from the first wire, the

second wire having a second substantially vertical surface, the first wire and the second wire are each horizontally disposed along side each first substantially vertical surface and the second substantially vertical surface, the one or more capacitor capacitances progressively reduced responsive to the first wire taper.

2. The layer, according to claim 1, Chiyoma further comprising at least one dielectric material disposed between the first substantially vertical surface and the second substantially vertical surface.

3. The layer, according to claim 1, Chiyoma show wherein the first wire is a signal wire.

4. The layer, according to claim 3, Chiyoma show wherein the second wire is a shielding wire.

5. The layer, according to claim 4, Chiyoma show wherein the first wire is tapered in progressively inward stepwise indentations away from the second wire along the first substantially vertical surface.

6. The layer, according to claim 5, Chiyoma show wherein the first wire is tapered in progressively inward stepwise indentations toward the second wire along another substantially vertical surface of the first wire.

7. The layer, according to claim 1, Chiyoma show wherein the first wire is a shielding wire, the shielding wire for a non-transitioning signal voltage, the non-transitioning signal voltage not transitioning form high to low and low to high logics levels during application of electrical energy to operate the integrated circuit.

8. The layer, according to claim 7, Chiyoma show wherein the second wire is a signal wire, the signal wire for a transitioning signal voltage, the transitioning signal voltage transitioning from high to low and low to high logic levels during application of the electrical energy to operate the integrated circuit.

9. The layer, according to claim 8, wherein the first wire is continuously tapered away from the second wire along the first substantially vertical surface.

10. The layer, according to claim 8, Chiyoma show wherein the first wire is continuously tapered toward the second wire.

11. Chiyoma (figures 1 to 14) specifically figure 3 show an integrated circuit conductive line, comprising: a plurality of loads **4**, the plurality of loads progressively reduced responsive to progressively reduced parasitic capacitance; a plurality of taps , a tap of the plurality of taps located between a pair of loads of the plurality of loads.

12. The integrated circuit conductive line, according to claim 11, Chiyoma show wherein load capacitance at the tap is substantially less than the parasitic capacitance at the tap location from a portion of the plurality of loads.
13. The integrated circuit conductive lines, according to claim 12, Chiyoma show wherein the load capacitance comprises transistor gate capacitance.
14. The integrated circuit conductive line, according to claim 13, Chiyoma show wherein the transistor gate capacitance is from a transistor formed with sub-quarter micron lithography.
15. The integrated circuit conductive line, according to claim 14, Chiyoma show wherein the plurality of loads are provided using tapered signal line.
16. The integrated circuit conductive lien, according to claim 15, Chiyoma show wherein the tapered signal line has a minimum width of one micron.
17. The integrated circuit conductive line, according to claim 15, Chiyoma show wherein the tapered signal line is a clock signal line.
18. The integrated circuit conductive line, according to claim 15, Chiyoma show wherein the tapered signal line is a delay line.
19. The integrated circuit conductive line, according to claim 14, Chiyoma show wherein the plurality of loads are provided using a tapered shielding line.
20. the integrated circuit conductive line, according to claim 19, Chiyoma show wherein the tapered shielding line is either a ground line or a source voltage line.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/775,773,644,665,776,e23.144,e23.152.e23.167.e27.141	9/13/06
Other Documentation: foreign patents and literature in 257/775,773,644,665,776,e23.144,e23.152.e23.167.e27.141	9/13/06
Electronic data base(s): U.S. Patents EAST	9/13/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
9/13/06